



三明學院

二〇二三年十二月

目 录

EDA

_____ ()

				2
			32	0
A				
B				
C	1.			
	2.			
	3.			i
	4.			

D					
E					
				5	
			4	0	6
			8	0	14
			8	0	8
			4	0	6
			5		6
			32	0	32
F	_____				
G				3	

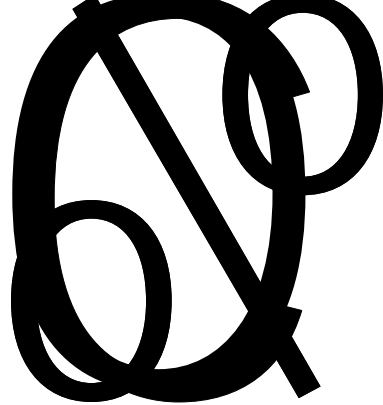
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					

	16					
	17					
	18					
H						
					1 2 3 4	
					1 2 3	
I	1.					2020 6
J						
K						

_____ ()

	EDA				
					2
			32		16
A	C				
B	<p>EDA (HDL) ASI C FPGA</p> <p>HDL SoC</p> <p>FPGA_Verilog HDL</p> <p>Verilog_HDL</p> <p>Verilog_HDL FPGA Verilog_HDL</p>				
	1. FPGA_Verilog HDL				

C	2. FPGA_Veril og HDL			
	3. FPGA_Veril og HDL			
	4. FPGA_Veril og HDL ;			
	5.			
D				
E				
			2	4
			2	4
			2	6
			2	4
			2	6
		0	6	6
		16	16	32



3

1

2

G

3

4

5

6

H

1 2 3 4

J	
K	

_____ ()

				2
			48	16
A				
B	fl i p chi p			
C	1. 2. 3. 4.			

D

2 0 2

E

ECOLOGY

	5		1 2 3 4			+
	6	EDA	1 2 3 4			+
H						
	10%	10 1 / 0.25/	9 0.5/ 0.5-1 10		1 2 3 4	
	30%				1 2 3 4	
	60%		+		1 2 3 4	
I	(1) (2)					
J						
K						

_____ ()

				2
			48	16
A				
B	Si P			
C	1. 2. 3. 4.			

D					
E					
	Si P		2	2	4
	Si P		2	4	6
	Si P		4	8	12
	Si P		4	8	12
	Si P		2	6	8
	Si P		2	4	6
			16	32	48
	F				

G				3	
	1	Si P	1 2 3 4	+	
	2	Si P	1 2 3 4	+	
	3	Si P	1 2 3 4	+	
4	Si P	1 2 3 4	+		

	5	Si P	1 2 3 4			+
	6	Si P	1 2 3 4			+
H						
	10%		10 1 / 0.25/	9 0.5/ 0.5-1 10		1 2 3 4
	30%					1 2 3 4
	60%			+		1 2 3 4
I	(1) (2)					
J						
K						

_____ ()

					2
			48		32
A					
B	PCB RFI C/MMIC EDA PCB PCB /				
C	1. 2. 3.				

	4.					
D						
E						
				2	2	4
				2	4	6
				4	4	12
				2	4	12
				4	6	8
				2	4	6
				0	8	8
			16	32	48	
F	_____					
G					3	
	1					
	2				+	
	3				+	

	4					+
	5					+
	6					+
	7					
H						
	30%				1 2 3 4	
	60%				1 2 3 4	
I						
J						
K						
